Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use several sheets if necessary)

Atty. Docket No. 98095DIV4	Serial No.: 10/008,653
Applicant Gonzales	
Filing Date November 9, 2001	Group 2815

U. S. PATENT DOCUMENTS

Examiner Initial		Document Number	Issue Date	Patentee	Class	Sub-Class	Filing Date
KPN		4,470,852	Sep. 11, 1984	Ellsworth			

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Examiner Initial		Document Number	Public. Date	County or Patent Office	Class	Sub-Class	Transl Y	Transl N

OTHER DOCUMENTS

(Including Author, Title, Date, Relevant Pages, Place of Publication)

KPN			Wolf et al. (Silicon Processing For The VLSI ERA, Volume 1: Process Technology, pp. 397-399, 1986)
Examiner MPQ			Date Considered 7/25/07

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Atty. Docket No. 98095DIV3	Serial No. 10/008,653
	Applicant Gonzalez et al.	
	Filing Date 11/9/01	Group

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Examiner Initial		Document Number	Issue Date	Patentee	Class	Sub-Class	Filing Date
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			Moravvej-Farshi, M. et al., "Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain," Solid-State Electronics, Vol. 30, No. 10, 1987, pp. 1053-62.
			Lynch, W. et al., "UPMOS-A New Approach to Submicron VLSI," Solid State Devices, 1988.
			Yamada, T. et al., "Spread/Source Drain (SSD) MOSFET Using Selective Silicon Growth for 64mbit DRAMs," 1989 IEDM, December 3-6, 1989, pp. 35-38.
			Shin, H. et al., "MOSFET Drain Engineering Analysis for Deep Submicron Dimensions: Part II - A New Structural Approach for Deep Submicron MOSFETs," SRC, November 1991.
			M. Togo et al., "A Gate-side Air-gap Structure (GAS) to Reduce the Parasitic Capacitance in MOSFET," 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 38-39.
			Makino, T. et al., "A Stacked Source Drain MOSFET Using Selective Epitaxy," Fujitsu Limited, Publication Date Unknown.
Examiner			Date Considered 7/25/07

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